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10/777,174	02/13/2004	Kenneth Koch II	10017911-3	4476

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,174	KOCH ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-12,14,16-18,22 and 24-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,16-18,22 and 30-32* is/are allowed.

6)☒ Claim(s) *1,3,7-11,24,27 and 28* is/are rejected.

7)☒ Claim(s) *12,25,26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 3 and 7-12 and 25-27 are objected to because of the following informalities:

Claim 1, lines 13-15, "of the first transistor, the capacitor being connected across the gate electrode of one of said transistors" should be changed to --of one of said transistors, the capacitor being connected across the gate electrode said one of said transistors-- since line 14 recites the capacitor being connected across the gate electrode of one of said transistors, so the recitation "of the first transistor" on line 13-14 must be changed to --of one of said transistor--, and "of one of" on line 14 must be changed to --of said one of--.

Claims 3, 7-12 and 25-27 are objected to because they include the informalities of claim 1.

Claim Rejections – 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 7-11, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki et al. (USP 5,694,065) in view of Love (USP 5,068,553).

With respect to claims 1, 3 and 27 Figure 2 of the Hamasaki et al. reference discloses a circuit which includes a first terminal (IN); a driver (50, 60) having a first transistor (PFET 50) and a second transistor (NFEF 60) each having a source drain path; output terminal (OUT); first (ground supply) and second (5V supply) opposite power supply terminals; and pulse shaping

circuitry (72, 74, Rn, Cn, 82, 84, Rp and Cp) for (a) causing the first and second source drain paths to be respectively (i) on and off while the voltage source has the first level (5V) and (ii) off and on while the voltage source (IN) has the second level (0V), and (b) preventing both source drain paths from being on simultaneously (lines 60 of Col. 5 to line 21 of Col. 6); wherein the pulse-shaping circuitry comprising a resistive element (resistor Rn) and a capacitor (Cn), the resistive element (Rn) being connected for supplying current to the capacitor (Cn) and the gate electrode of the first transistor (PFET 50), the capacitor (Cn) being connected a gate electrode of the first transistor (PFET 50) and the first power supply terminal (ground supply), the first power supply terminal (ground supply) being connected for supplying current to the source drain path of the second transistor (NFET 60) while the second transistor (NFET 60) is on. Figure 2 of the Hamasaki et al. reference does not disclose that the first capacitor (Cn) comprising an n-channel field effect device (i.e., transistor having a conductivity type opposite to the conductivity type of the PFET first transistor 50). However, the Love reference discloses that a capacitor is easily formed by using an NMOS transistor that has its drain and its source connected together (see capacitor 26 in Figure 1, or capacitor 80 in Figure 3). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the Hamasaki reference to use specific capacitor-connected NMOS transistor (as taught by the by the Love reference) for broad capacitor elements in the circuit of Figure 2 of the Hamasaki reference (i.e., each of the capacitors Cn and Cp in Figure 2 is implemented by a capacitor-connected NMOS transistor) for the purpose of easily integrated the circuit. Thus, this modification/combination meets the limitations of claim 1 because the capacitor (Cn) being a FET device (n-channel FET as discussed) having a conductivity type opposite from the of the

first of the transistors (i.e., PFET 50). Note that all the elements (resistor Rn, capacitor Cn, PFET 50 and NFET 60) are included in an integrated circuit chip (claim 3), and the voltage source (IN) has transitions in both directions between the first and second levels (see lines 60 of Col. 5 to line 21 of Col. 6, Hamasaki et al.).

With respect to claims 7-9, Figure 2 of Hamasaki et al. in the above combination shows the pulse shaping circuitry including the a switching circuit (72, 74) having an input terminal and an output terminal, the output terminal of the switching circuit being connected so current can flow via a DC path between (a) the first power supply terminal (ground) and (b) the capacitor and the gate electrode of the first transistor, wherein the DC path including the resistive element Rn (i.e., when transistor 74 is ON, then current flows through a DC path from ground through the source-drain of transistor 74 and through the resistor Rn to the gate of PFET 50 and capacitor Cn); wherein the pulse-shaping circuitry comprising an inverter (72, 74) having FETs, wherein all the FETs of the inverter are included in an integrated circuit chip including a resistor (Rn) comprising the resistive element (Rn).

For claims 10 and 11, for broadest reasonable interpretation, the combination of elements 72, 74 and Rn forms an inverter, and thus the output of inverter is signal D01, so it meets the limitation the resistive element included in the inverter, wherein inverter also comprises another PFET (72) and another NFET (74).

With respect to claim 24, this claim is rejected for the similar reasons as discussed in claims 1, 3 and 7-11 above.

With respect to claim 28, Figure 2 of the Hamasaki et al. reference discloses a circuit which includes a first terminal (IN); a driver (50, 60) having a first transistor (PFET 50) and a

second transistor (NFEF 60); output terminal (OUT); pulse shaping circuitry (72, 74, Rn, Cn, 82, 84, Rp and Cp) comprising a resistive element (resistor Rn) and a capacitor (Cn); first (5V power supply) and second (ground supply) opposite power supply terminals for respectively providing first and second DV voltages (5V and 0V). Figure 2 of the Hamasaki et al. reference does not disclose that the first capacitor (Cn) comprising an n-channel field effect device (i.e., transistor having a conductivity type opposite to the conductivity type of the PFET first transistor 50). However, the Love reference discloses that a capacitor is easily formed by using an NMOS transistor that has its drain and its source connected together (see capacitor 26 in Figure 1, or capacitor 80 in Figure 3). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the Hamasaki reference to use specific capacitor-connected NMOS transistor (as taught by the by the Love reference) for broad capacitor elements in the circuit of Figure 2 of the Hamasaki reference (i.e., each of the capacitors Cn and Cp in Figure 2 is implemented by a capacitor-connected NMOS transistor) for the purpose of easily integrated the circuit. Thus, this modification/combination meets the limitations of claim 28 because the capacitor (Cn) being a FET device (n-channel FET as discussed) having a conductivity type opposite from the of the first of the transistors (i.e., PFET 50) and including first and second electrodes connected between the gate electrode of the first of the transistors and the power supply terminal (ground) for supplying current directly to the source drain path of the second of the transistors (i.e., NFET 60).

Allowable Subject Matter

4. Claims 14, 16-18, 22 and 30-32 are presently allowed over the prior art.

5. Claims 12, 25, 26 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the minor informalities set forth above (for claims 12, 25 and 26).

Response to Arguments

6. Applicant's arguments filed on 12/7/06 have been fully considered but they are not persuasive.

Applicant argues that Col. 5, lines 32-59 of Hamasaki et al. discussed the structure of capacitors Cn and Cp extensively, wherein Cn and/or Cp is formed by using conductor wiring or as a metal coating and a dielectric coating, and that there is no indication from the applied art that substituting the Love NMOS device for capacitor Cn and/or Cp would facilitate manufacture of the Hamsaki et al. integrated circuit. However, this argument is not persuasive because it is old and well known in the art that one way to form a capacitor is by using a transistor where its drain and source connected together (for example, as taught by Love, where NMOS 26 in Figure 1, or NMOS 80 in Figure 3). Thus, one skill in the art can easily modify the Hamasaki et al. by using an NMOS transistor, as taught by Love, to form a capacitor for Cn and/or Cp because the use of NMOS transistor to form a capacitor is old and well known, and the circuitry still functions equivalent.

Applicant also argues that the Examiner, in making this rejection, has cast about to find circuits that are similar to applicants' circuit and, through the use of hindsight, has combine the references. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on

obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Note that, in this case, Love clearly teaches a capacitor is formed by using NMOS transistor where its drain and source connected together, and thus, one skill in the art would easily modify the Hamasaki et al. by using an NMOS transistor, as taught by Love, to form a capacitor for Cn and/or Cp because the use of NMOS transistor to form a capacitor is old and well known, and the circuitry still functions equivalent.

Note that, in modification of the Hamasaki et al. reference by using NMOS capacitor as taught by Love for each of the capacitors Cn and Cp as discussed above in the rejection of claim 1, then it is clearly that capacitor modified Cn comprises an NMOS which is opposite to the conductivity of the first transistor (PMOS 50).

Applicant further argues that in Love, the gates of the PFET and NFET devices are connected to a common terminal, in other words, the portion of the Love circuitry including PFET 82 and NFET 84, that are driven in parallel by a single voltage at terminal 76, is entirely different from the configuration of Hamasaki et al., wherein PFET 50 and NFET 60 are separately driven by different inverters and low pass filter circuits, and thus one of ordinary skill in the art would not have looked to Love NMOS as a replacement for capacitor Cn of Hamasaki et al. However, this argument is not persuasive because the modification of Hamasaki et al. would only require to fabricate the capacitors Cn and Cp each by using an NMOS device as taught by Love that a capacitor is formed by using an NMOS where its drain and source are

connected together. Thus, one skill in the art can easily modify the Hamasaki et al. by using an NMOS transistor, as taught by Love, to form a capacitor for Cn and/or Cp because the use of NMOS transistor to form a capacitor is old and well known, and the circuitry still functions equivalent.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER